CLAIMS

What is claimed is:

1. A signal generator circuit comprising:

a spreading profile controller adapted to calculate, in real time, a divisor value in accordance with a spreading profile characterized by a function; and

a fractional divider dividing an output signal of the signal generator circuit by the divisor value;

wherein the signal generator is adapted to adjust, based on the divided output signal and a reference signal, a frequency of the output signal of the signal generator circuit; and

wherein the spreading profile controller is adapted to calculate one or more new divisor values in accordance with the spreading profile, and

wherein the spreading profile controller calculates each of the one or more new divisor values so as to vary the frequency of the output signal of the signal generator circuit in accordance with the spreading profile, and wherein the output signal of the signal generator circuit is generated without discontinuities in the varied frequency.

2. The invention as recited in claim 1, wherein the spreading profile controller varies the frequency of the output signal so as to switch the frequency from a first value to a second value without an observed discontinuity.

3. The invention as recited in claim 2, wherein the spreading profile is a triangular profile.

4. The invention as recited in claim 3, wherein the spreading profile controller calculates the new divisor value by:

(1) testing whether the spreading profile is up spreading or down spreading;

if the spreading profile is up spreading, then

(2) adding a slope value to the divisor to generate the new divisor; and

if the spreading profile is down spreading, then

(3) subtracting the slope value from the divisor to generate the new divisor.

5. The invention as recited in claim 1, wherein the spreading profile controller receives a signal indicating whether spreading is enabled and, if spreading is not enabled, suspends calculating divisor values.

6. The invention as recited in claim 1, wherein the fractional divider is adapted to implement a fractional accumulation method.

7. The invention as recited in claim 6, wherein the fractional divider comprises:

an accumulator storing the divisor value as an integer component and as a fractional component; and

a counter adapted to divide the output signal by the integer component,

wherein the counter selects, as the divided output signal, a phase of the counter based on the fractional component.

8. The invention as recited in claim 7, wherein the fractional divider comprises a combiner adapted to update the integer component and the fractional component based on the new divisor value.

9. The invention as recited in claim 1, wherein the spreading profile is one of a plurality of spreading profiles, and the spreading profile controller is adapted to select one of the plurality of spreading profiles.

10. The invention as recited in claim 1, wherein the signal generator is either a phase-locked loop (PLL) or a delay-locked loop (DLL).

11. A method of implementing a signal generator comprising the steps of:

(a) calculating a divisor value in real time in accordance with a spreading profile characterized by a function;

(b) dividing an output signal of the signal generator by the divisor value;

(c) adjusting, based on the divided output signal and a reference signal, a frequency of the output signal of the signal generator;

(d) calculating a new divisor value in accordance with a spreading profile; and

(e) repeating steps (a) through (d) so as to vary the frequency of the output signal of the signal generator in accordance with the spreading profile without discontinuities in the slewed frequency.

12. The invention as recited in claim 11, wherein step (e) further comprises the step of:

varying the frequency of the output signal so as to switch the frequency from a first value to a second value without an observed discontinuity.

13. The invention as recited in claim 11, wherein the spreading profile is a triangular profile.

14. The invention as recited in claim 13, wherein step (d) calculates the new divisor value by the steps of:

(d1) testing whether the spreading profile is up spreading or down spreading;

if the spreading profile is up spreading, then

(d2) adding a slope value to the divisor to generate the new divisor; and

if the spreading profile is down spreading, then

(d3) subtracting the slope value from the divisor to generate the new divisor.

15. The invention as recited in claim 11, further comprising the step of testing whether spreading is enabled and, if spreading is enabled, performing steps (a) through (e) and, if spreading is not enabled, suspending steps (a) through (e).

16. The invention as recited in claim 11, wherein, for step (b), the dividing step includes the step of implementing a fractional accumulation method.

17. The invention as recited in claim 16, wherein the fractional accumulation method step comprises the steps of:

(b1) separating the divisor value into an integer component and a fractional component;

(b2) dividing, with a counter, the output signal by the integer component; and

(b3) selecting, as the divided output signal, a phase of the counter based on the fractional component.

18. The invention as recited in claim 17, wherein, for step (d), the integer component and the fractional component are updated based on the new divisor value.

19. The invention as recited in claim 11, wherein, for step (a), the spreading profile is one of a plurality of spreading profiles, and step (a) further comprises the step of selecting one of the plurality of spreading profiles.

20. The invention as recited in claim 11, wherein the method implements a signal generator as either a phase-locked loop (PLL) or a delay-locked loop (DLL).